

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE



Membership Publications/Services Standards Conferences Careers/Jobs

**IEEE Xplore®**  
 RELEASE 1.7

 Welcome  
 United States Patent and Trademark Office


» Se

[Help](#) [FAQ](#) [Terms](#) [IEEE Peer Review](#)
[Quick Links](#)

Welcome to IEEE Xplore®

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

Print Format

Your search matched **14** of **1045422** documents.A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.**Refine This Search:**

You may refine your search by editing the current search expression or enter a new one in the text box.

programmable bist

Search

☐ Check to search within this result set**Results Key:****JNL** = Journal or Magazine **CNF** = Conference **STD** = Standard**1 A programmable BIST core for embedded DRAM**

Chih-Tsun Huang; Jing-Reng Huang; Chi-Feng Wu; Cheng-Wen Wu; Tsin-Yua Chang;

Design & Test of Computers, IEEE , Volume: 16 , Issue: 1 , Jan.-March 1999  
Pages:59 - 70
[\[Abstract\]](#) [\[PDF Full-Text \(168 KB\)\]](#) **IEEE JNL**
**2 A programmable BIST for embedded SDRAM**

Zhang, M.; Tao, D.; Wei, B.;

VLSI Technology, Systems, and Applications, 2001. Proceedings of Technical Papers. 2001 International Symposium on , 18-20 April 2001  
Pages:244 - 248
[\[Abstract\]](#) [\[PDF Full-Text \(332 KB\)\]](#) **IEEE CNF**
**3 Magnetically programmable bistable laser diode with ferromagnetic layer**

Zaets, W.; Ando, K.;

Photonics Technology Letters, IEEE , Volume: 13 , Issue: 3 , Mar 2001  
Pages:185 - 187
[\[Abstract\]](#) [\[PDF Full-Text \(80 KB\)\]](#) **IEEE JNL**
**4 A programmable BIST architecture for clusters of multiple-port SRA**

Benso, A.; Di Carlo, S.; Di Natale, G.; Prinetto, P.; Lobetti Bodoni, M.;

Test Conference, 2000. Proceedings. International , 3-5 Oct. 2000  
Pages:557 - 566
[\[Abstract\]](#) [\[PDF Full-Text \(668 KB\)\]](#) **IEEE CNF**

---

**5 A P1500-compatible programmable BIST approach for the test of embedded flash memories**

*Bernardi, P.; Rebaudengo, M.; Reorda, M.S.; Violante, M.;*

Design, Automation and Test in Europe Conference and Exhibition, 2003 , 2003  
Pages:720 - 725

[\[Abstract\]](#) [\[PDF Full-Text \( KB\)\]](#) **IEEE CNF**

---

**6 Programmable BIST space compactors**

*Ivanov, A.; Tsuji, B.K.; Zorian, Y.;*

Computers, IEEE Transactions on , Volume: 45 , Issue: 12 , Dec. 1996  
Pages:1393 - 1404

[\[Abstract\]](#) [\[PDF Full-Text \(1324 KB\)\]](#) **IEEE JNL**

---

**7 Exploiting programmable bist for the diagnosis of embedded memory cores**

*Appello, D.; Bernardi, P.; Fudoli, A.; Rebaudengo, M.; Reorda, M.S.; Tancorre, M.; Violante, M.;*

Test Conference, 2003. Proceedings. ITC 2003. International , Volume: 1 , September 30-Oct. 2, 2003  
Pages:379 - 385

[\[Abstract\]](#) [\[PDF Full-Text \(756 KB\)\]](#) **IEEE CNF**

---

**8 A P1500 compliant programmable BistShell for embedded memories**

*Koranne, S.; Wouters, C.; Waayers, T.; Kumar, S.; Beurze, R.; Visweswaran, S.;*  
Memory Technology, Design and Testing, IEEE International Workshop on , 2001 , 6-7 Aug. 2001

Pages:21 - 27

[\[Abstract\]](#) [\[PDF Full-Text \(468 KB\)\]](#) **IEEE CNF**

---

**9 Programmable memory BIST and a new synthesis framework**

*Zarrineh, K.; Upadhyaya, S.J.;*

Fault-Tolerant Computing, 1999. Digest of Papers. Twenty-Ninth Annual International Symposium on , 15-18 June 1999  
Pages:352 - 355

[\[Abstract\]](#) [\[PDF Full-Text \(152 KB\)\]](#) **IEEE CNF**

---

**10 A new framework for automatic generation, insertion and verification of memory built-in self test units**

*Zarrineh, K.; Upadhyaya, S.J.;*

VLSI Test Symposium, 1999. Proceedings. 17th IEEE , 25-29 April 1999  
Pages:391 - 396

[\[Abstract\]](#) [\[PDF Full-Text \(172 KB\)\]](#) **IEEE CNF**

---

**11 Programmable built-in self-testing of embedded RAM clusters in system-on-chip architectures**

*Benso, A.; Di Carlo, S.; Di Natale, G.; Prinetto, P.; Bodoni, M.L.;*

Communications Magazine, IEEE , Volume: 41 , Issue: 9 , Sept. 2003  
Pages:90 - 97

[\[Abstract\]](#) [\[PDF Full-Text \(571 KB\)\]](#) IEEE JNL

---

**12 Neighborhood pattern-sensitive fault testing and diagnostics for random-access memories**

*Kuo-Liang Cheng; Ming-Fu Tsai; Cheng-Wen Wu;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on , Volume: 21 , Issue: 11 , Nov. 2002

Pages:1328 - 1336

[\[Abstract\]](#) [\[PDF Full-Text \(648 KB\)\]](#) IEEE JNL

---

**13 A 16 GB/s, 0.18  $\mu$ m cache tile for integrated L2 caches from 256 KiB**

*Miller, J.L.; Conary, J.; DiMarco, D.;*

VLSI Circuits, 2000. Digest of Technical Papers. 2000 Symposium on , 15-17 2000

Pages:228 - 231

[\[Abstract\]](#) [\[PDF Full-Text \(276 KB\)\]](#) IEEE CNF

---

**14 Design and test of a 9-port SRAM for a 100 Gb/s STS-1 switch**

*Gibbins, R.; Adams, R.D.; Eckenrode, T.; Ouellette, M.; Yuejian Wu;*

Memory Technology, Design and Testing, 2002. (MTDT 2002). Proceedings of 2002 IEEE International Workshop on , 10-12 July 2002

Pages:83 - 87

[\[Abstract\]](#) [\[PDF Full-Text \(478 KB\)\]](#) IEEE CNF

---

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#) | [Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#) | [No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2004 IEEE — All rights reserved